IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

NEVILL et al.   Atty. Ref.: 550-242

Serial No. Unknown   Group:

Filed: June 25, 2001   Examiner:

For: RESTARTING TRANSLATED INSTRUCTIONS

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June 25, 2001

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

PRELIMINARY AMENDMENT

In order to place the above-identified application in better condition for examination,

please amend the application as follows:

IN THE CLAIMS

Please cancel claims 18, 19 and 20 without prejudice or disclaimer.

Please substitute the following amended claims for corresponding claims previously

presented. A copy of the amended claims showing current revisions is attached.

3. (Amended) Apparatus as claimed in claim 1, wherein said translator output signals include

control signals that control operation of said processor core and match control signals produced

on decoding instructions of said first instruction set.

4. (Amended) Apparatus as claimed in claim 1, wherein said translator output signals include control signals that control operation of said processor core and specify parameters not specified by control signals produced on decoding instructions of said first instruction set.

5. (Amended) Apparatus as claimed in claim 1, wherein said restart logic is part of said instruction translator.

6. (Amended) Apparatus as claimed in claim 1, wherein said restart logic stores a pointer to a restart location within instructions of said second instruction set that are being translated, said pointer being advanced upon execution of said final operation.

8. (Amended) Apparatus as claimed in claim 1, wherein instructions of said second instruction set specify operations to be executed upon stack operands held in a stack and said input variables include input stack operands.

10. (Amended) Apparatus as claimed in claim 8, wherein any stack operands added to said stack by execution of said at least one instruction of said second instruction are not added until after execution of said final operation has commenced.

11. (Amended) Apparatus as claimed in claim 1, wherein said input variables include system state variables not specified within said second instruction.

12. (Amended) Apparatus as claimed in claim 1, wherein said processor has a register bank containing a plurality of registers and instructions of said first instruction set execute operations upon register operands held in said registers.

15. (Amended) Apparatus as claimed in claim 1, wherein said instructions of said second instruction set are Java Virtual Machine instructions.
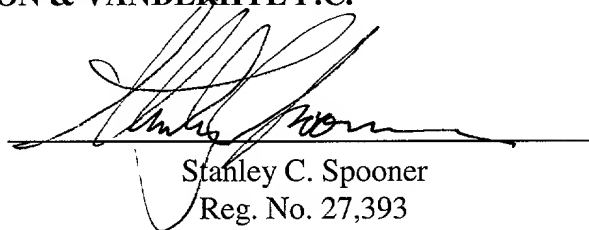
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REMARKS

The above amendments are made to place the claims in a more traditional format.

Attached hereto is a marked-up version of the changes made to the claims by the current

amendment. The attached pages are captioned "**Version With Markings To Show Changes**

Made."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

3. (Amended) Apparatus as claimed in [any one of claims 1 and 2] claim 1, wherein said

translator output signals include control signals that control operation of said processor core and

match control signals produced on decoding instructions of said first instruction set.

4. (Amended) Apparatus as claimed in [any one of claims 1, 2 and 3] claim 1, wherein said

translator output signals include control signals that control operation of said processor core and

specify parameters not specified by control signals produced on decoding instructions of said

first instruction set.

5. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein said

restart logic is part of said instruction translator.

6. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein said

restart logic stores a pointer to a restart location within instructions of said second instruction set

that are being translated, said pointer being advanced upon execution of said final operation.

8. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein

instructions of said second instruction set specify operations to be executed upon stack operands

held in a stack and said input variables include input stack operands.

10. (Amended) Apparatus as claimed in [any one of claims 8 and 9] claim 8, wherein any stack

operands added to said stack by execution of said at least one instruction of said second

instruction are not added until after execution of said final operation has commenced.

11. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein said

input variables include system state variables not specified within said second instruction.

12. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein said

processor has a register bank containing a plurality of registers and instructions of said first

instruction set execute operations upon register operands held in said registers.

15. (Amended) Apparatus as claimed in [any one of the preceding claims] claim 1, wherein said

instructions of said second instruction set are Java Virtual Machine instructions.

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